CLAIMS

We claim:

1. An integrated circuit chip comprising:

an array of pads, said pads including signal I/O, power and power return pads;

a plurality of I/O cells each being connected to one of said I/O pads by I/O signal wiring in one or more wiring layers; and

a plurality of ESD protection devices, each of said plurality of ESD protection devices being connected to one of said array of pads by a metal line, said metal line meeting an ESD width constraint and having a resistance below an ESD resistance constraint.

2. The integrated circuit chip of Claim 1, wherein the plurality of ESD protection devices comprises:

an ESD protect device in each of said plurality of I/O cells connected between an I/O circuit in said I/O cell and one of said I/O signal pads.

3. The integrated circuit of claim 2 wherein each said ESD protect device is further connected to power rails and power return rails connected to said circuit.

4. The integrated circuit chip of claim 3, wherein the plurality of ESD protection devices comprises:

an ESDxx cell connected between power rails and power return rails for at least two different power supplies.

5. The integrated circuit chip of claim 4 further comprising:

a plurality of ESDxx cells, each of said plurality of ESDxx cells being associated with a group of I/O cells.

6. The integrated circuit chip of claim 5 further comprising:

a plurality of said I/O signal lines being designated as unused, said unused I/O signal lines being connected to one of said power or power return rails.

7. A chip design method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints; and,

e) checking said wired integrated circuit.

8. The method of claim 7, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

9. The method of claim 8, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including a connection to power rail or to a power return rail.

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10. The method of claim 8, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including an ESD protect device.

11. The method of claim 8, wherein the generating step (d) comprises the step of:

i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

12. The method of claim 11, wherein the checking step (e) comprises checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints.

13. A chip design method comprising the steps of:

a) retrieving a power route pattern instruction;

b) identifying power and power return connections;

c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction; and

d) checking said wired integrated circuit.

14. The method of claim 13, wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a power rail or to a power return rail.

15. The method of claim 13, wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a cell including an ESD protect device.

16. The method of claim 13, wherein the routing step (c) includes the steps of:

i) providing an ESDxx cell; and

ii) connecting said ESDxx cell between power rails and power return rails for at least two different power supplies.

17. A chip design method comprising the steps of:

a) retrieving I/O and ESDxx cell identifications and placement constraints;

b) providing a plurality of ESDxx cells for placement;

c) placing each of said plurality of ESDxx cells with a group of I/O cells;

d) connecting each said placed ESDxx cell between power rails and power return rails for at least two different power supplies; and,

e) checking said wired integrated circuit.

18. A system for integrated circuit chip design comprising:

means for retrieving net constraints from technology data;

means for placing a plurality of I/O cells; and

means for connecting each of said placed I/O cells to I/O cells to an I/O pad according to said retrieved net constraints.

19. The system of claim 18, wherein said retrieved constrains include power bussing constraints, said system further comprising:

means for routing power and power return connections according to said power bussing constraints.

20. The system of claim 18, further comprising:

means for grouping I/O cells; and

means for placing an ESDxx cell with each group of I/O cells.